

Automated Verification of UML State Machines

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1 Context

The Unified Modeling Language (UML) [2] has become the dominant modeling language in many industrial areas such as software engineering. In particular, UML state machines are a widely used formalism including a precise graphical representation, and allowing to specify the behavior of concurrent systems. Their syntax provides powerful constructs, such as concurrency, hierarchy, sequential and parallel behavior.

In order to reduce the costs induced by design issues, it is crucial to detect model-level errors in the initial phase of software development. Errors appearing as early as the modeling phase of a project have dramatic time-consuming and cost-consuming consequences: It is only after finishing the implementation and verifying it or testing it with respect to the desired requirements that the error can be found, and the whole process, including the modeling, has to be restarted from the beginning.

Although widely used in the industry, UML is only given an informal semantics. As a consequence, UML is not directly suitable for formal verification methods, and needs to be given a formal semantics. We are interested in associating a semantics to UML state machines, and developing formal methods for modeling and verifying state machines, in order to detect potential errors as early as the modeling phase of a project.

2 Internship Proposal

UML state machines are given an informal description in the official specification [2], but no formal semantics is defined, thus preventing the application of formal techniques of verification. This internship first consists in associating a formal operational semantics to UML state machines, following as much as possible the informal semantic indications given in the specification [2]. We aim at considering a set of constructs as large as possible, and including at least the constructs studied in [4] and [1], in particular hierarchical aspects, join, fork, history pseudo states, and entry and exit points. Then, a semantics will be defined by associating to each elementary syntactical construct a formal definition. It would also be interesting to consider the timed aspects of UML state machines, which are essential for modeling real time systems. According to [2], actions in UML can be constrained by timing constraints, of the form "at" or "before" a time duration or interval.

A second step will consist in implementing the semantics into the PAT model checker [3]. This tool is an efficient model checker implemented in C# with a graphical interface able to verify real time systems, and other formalisms. Its architecture allows the addition of new formalisms (such as UML state machines) easily. This will allow us to perform automated verification on UML state machines.

3 Conditions

Applicants should be students in Master 2, and be highly motivated. Knowledge in UML and C# would be appreciated, but not compulsory. The internship takes place at LIPN (Laboratoire d'Informatique de Paris Nord) in the University of Paris 13 (Villetaneuse, 20 minutes from Paris Gare du Nord), for about 3 to 6 months preferably during spring and summer 2012, although other periods may be possible as well.

Standard monthly salary: 430 euros.

4 Contact

Please address applications and possible questions to Étienne André, Christine Choppy and Kais Klai, by email only, and mention which subject you are interested in.

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References

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4. S. Zhang and Y. Liu. An automatic approach to model checking UML state machines. In *Fourth International Conference on Secure Software Integration and Reliability Improvement Companion, SSIRI-C '10*, pages 1–6. IEEE Computer Society, 2010.